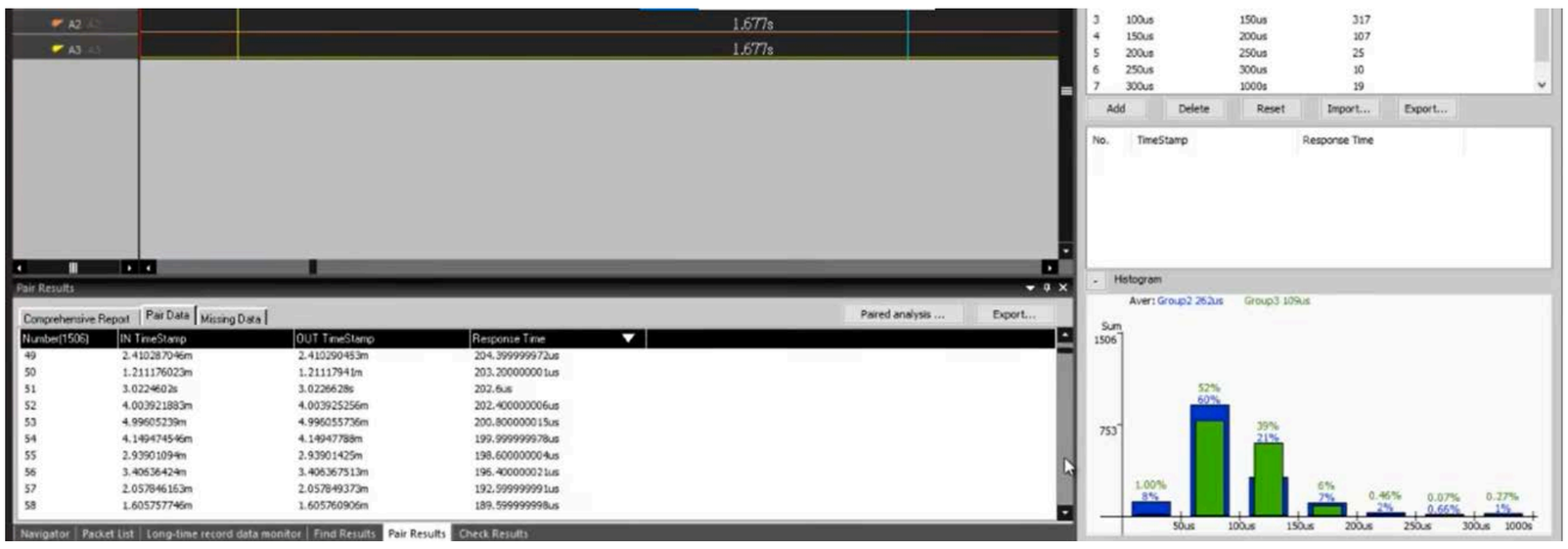
ZEROPLUS

ProCision

Show Signals' Latency & Packets Loss

The Automated Expert for Intel / AMD CPU Power-on Sequence & Stability Verification

STOP MANUAL DEBUGGING.



Process 10,000 data points in under 90 minutes.

Purpose-built for motherboard and embedded development, ProCision automated correlation engine identifies elusive anomalies in seconds, ensuring you stay ahead of the competition.

32-CHANNEL

256 MB PER CHANNEL

130+ PROTOCOL DECODER

SPECIFICATION

TECHNICAL SPECIFICATIONS

System & Interface

Operating System	Windows 11 / 10 / 8.1 / 7
PC Interface	USB 3.0 (Plug & Play)
Power Consumption	3W Max. (USB Bus-Powered)
Language Support	English / Traditional Chinese / Simplified Chinese

Hardware Performance

Channels	32 Channels
Max. Sampling Rate	2GHz / 8CH
Total Memory	8 Gbits
Input Impedance	200 kΩ / 7pF
Input Voltage Range	-30V to +30V (DC)
Threshold Range	-6V to +6V (Reference Voltage)

Physical & Environmental

Dimensions (L x W x H)	125 x 92 x 25 mm
Weight	170 g
Operating Temperature	5°C to 40°C (41°F to 104°F)

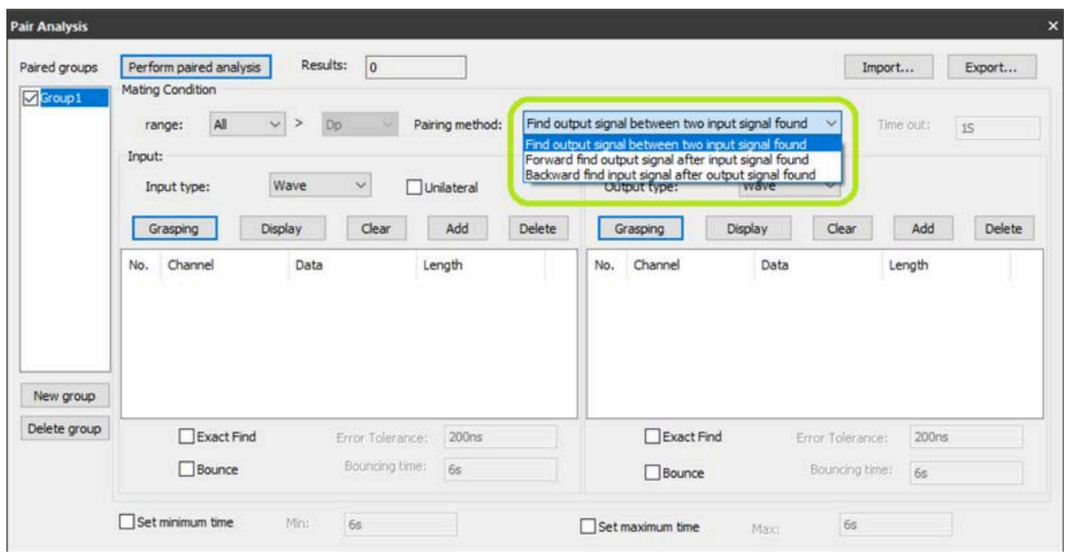
Compliance & Warranty

Certifications	FCC / CE / RoHS / REACH / WEEE
Warranty	2-Year Limited Warranty

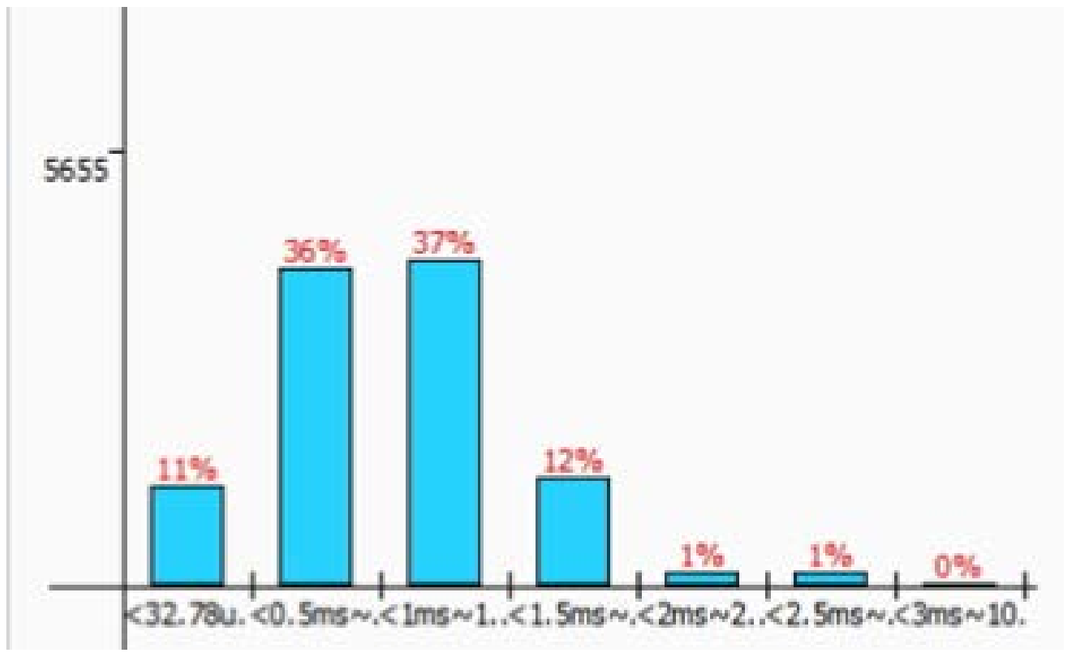
INSTRUMENT INSIGHT ENGINE

Advanced Big Data Integration for Instrumentation

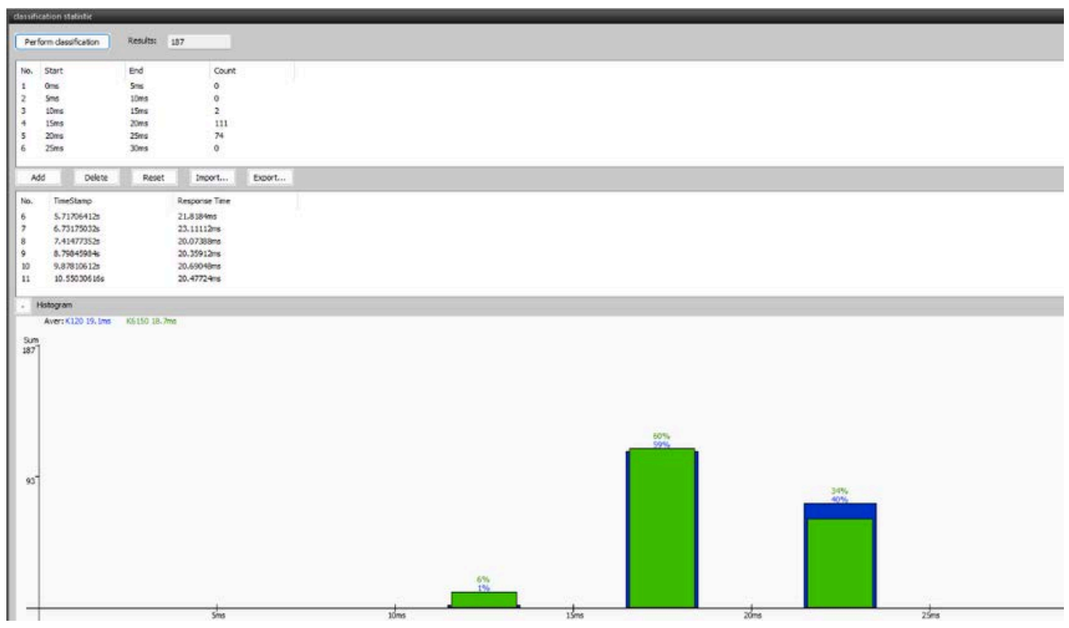
- Hardware-Embedded Analytics: Unlike traditional software-only solutions, our big data processing is natively embedded within the instrumentation domain.
- Dual-Path & Multi-Level Search: Utilizes proprietary Input/Output and multi-level search algorithms to efficiently filter critical datasets from long-term signal recordings.
- Automated Timing Extraction: Processes raw signals to generate precise timing information essential for engineering validation.
- Statistical Ranking & Analysis: Integrated software performs automated statistical analysis and dataset ranking, providing a complete end-to-end data insights workflow.



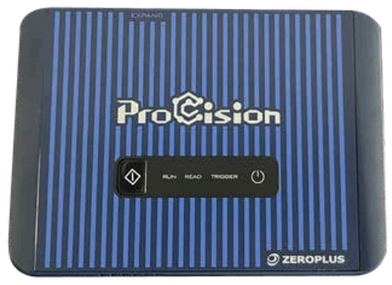
Dual-Path & Multi-Level Search
Software Interface



Automated Timing Extraction
Software Interface

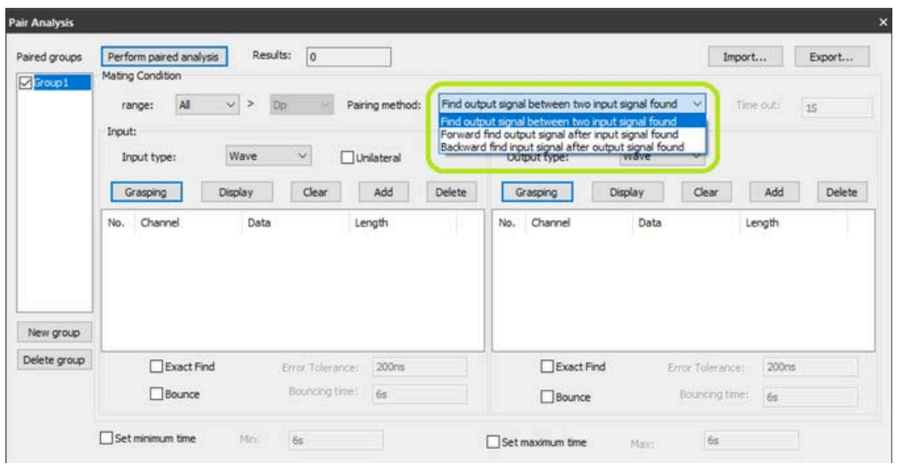


Statistical Ranking & Analysis
Software Interface

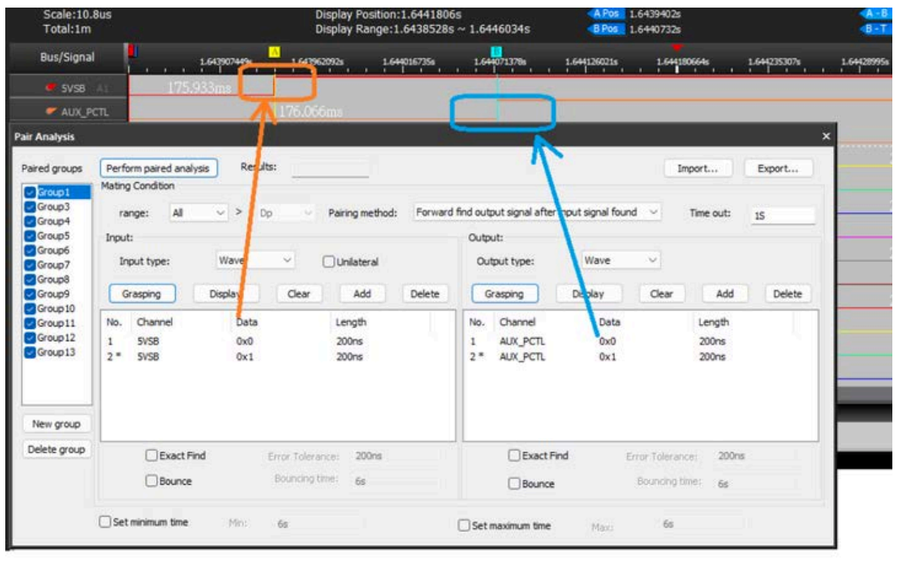
	 **LAP-C Pro 32256**	 **ProCision**
Market Price	3,600	10,000
Channel	32	
Memory per channel	8G(Max), 256M per channels	
Sample Rate (State)	250MHz	
Sample Rate (Timing)	Max.2GHz 500MHz/32CH 1GHz/16CH 2GHz/8CH	
Sample Rate (LTR)	200 MHz/ 200MByte	
Capability	USB2.0 module、10/100 Ethernet module	
Auto-Pairing	X	V
Timing Profiling	X	V
Compliance Validation (PASS/FAIL)	X	V

KEY SPECIFICATIONS

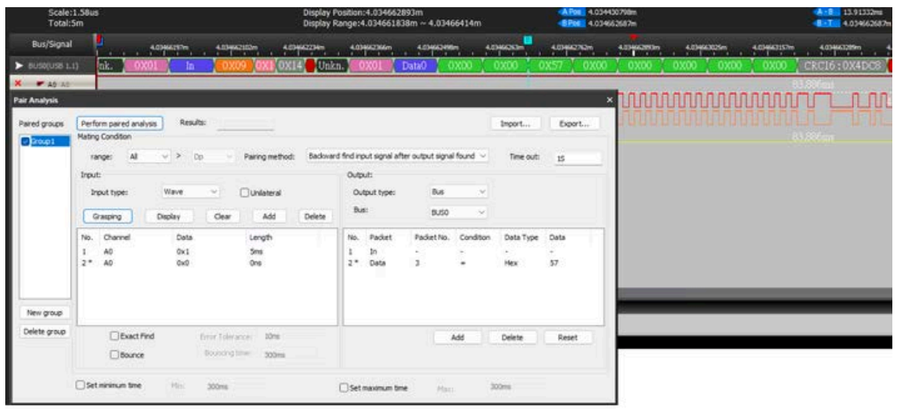
AUTO-PAIRING



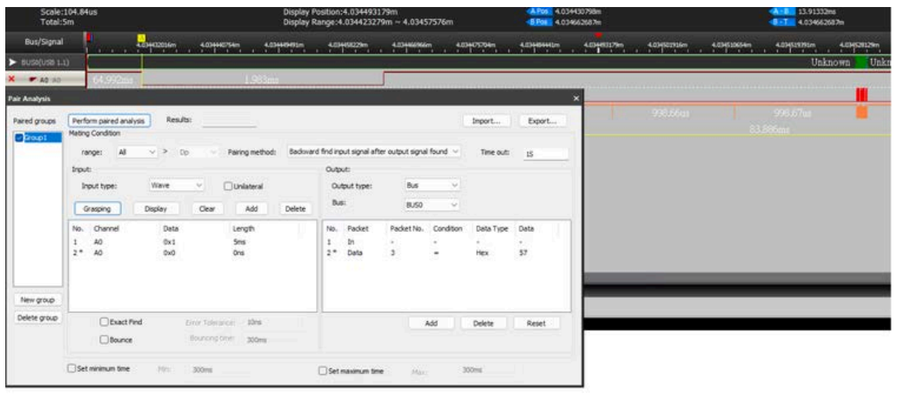
To precisely pinpoint complex signal transmission anomalies, our system offers three advanced pairing methods to synchronize input and output logic flows:



1. Process-Oriented Correlation (FSM Timing Decoding Mode)
This mode is defined as "Finite State Machine (FSM) Timing Decoding." Instead of using a fixed starting point, the system utilizes a predefined "Event Sequence Template" to automatically detect and pair I/O activities that match specific sequential logic within long-term data recordings.
Key Application: Used for complex "event-flow" analysis, such as monitoring entire Power-up/Down sequences or multi-stage bus handshaking protocols.



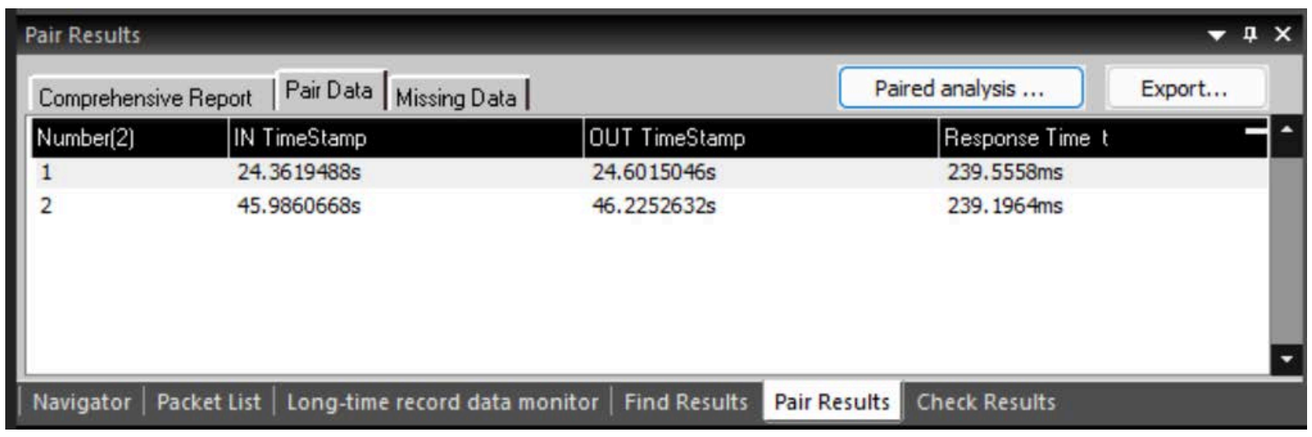
2. Upstream-to-Downstream Verification (Functional Response Mode)
This mode is defined as "Functional Response Validation." The system uses a valid trigger edge at the Input Port as the starting reference point. It then scans forward (positive delay) along the timeline to detect and monitor status changes at the Output Port.
Key Application: Used for forward-timing convergence analysis to measure system latency and ensure compliance with functional response specifications.



3. Downstream-to-Upstream Traceability (Root Cause Analysis Mode)
This mode is defined as "Root Cause Analysis." The system designates a specific logical transition or pulse at the Output Port as the T-Zero reference point. It then automatically scans backward (negative delay) along the timeline to retrieve signals from the Input Port that satisfy predefined logical conditions.
Key Application: Used for reverse-engineering signal triggers to verify which input event precisely caused a specific output response.

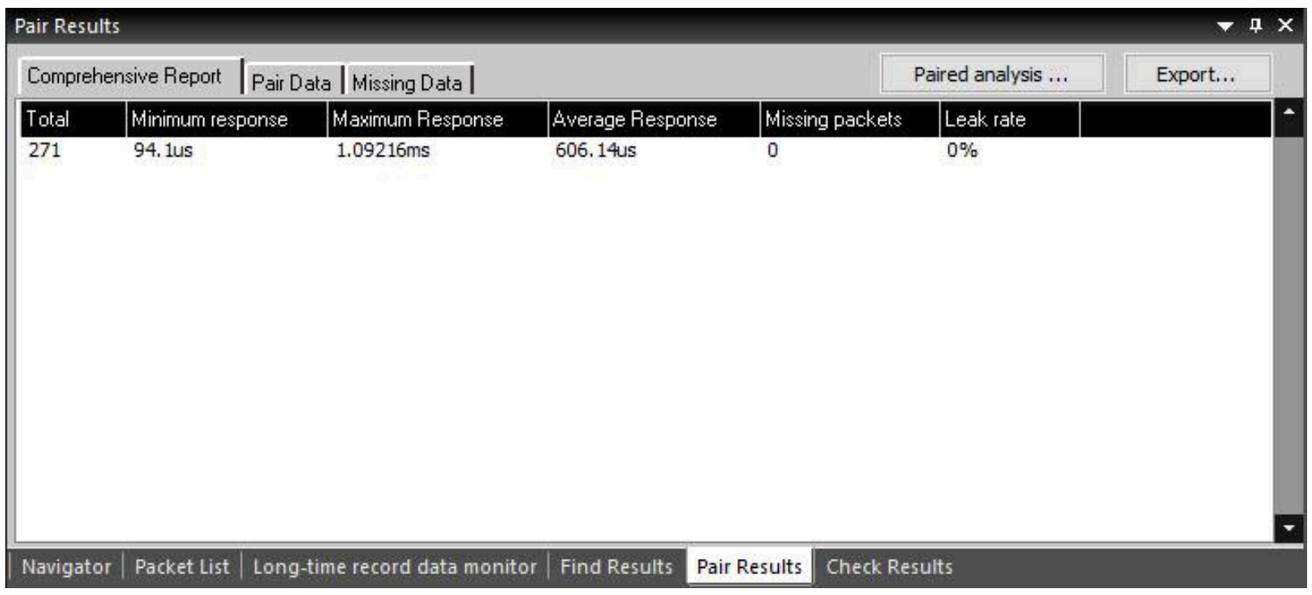
KEY SPECIFICATIONS

TIMING PROFILING

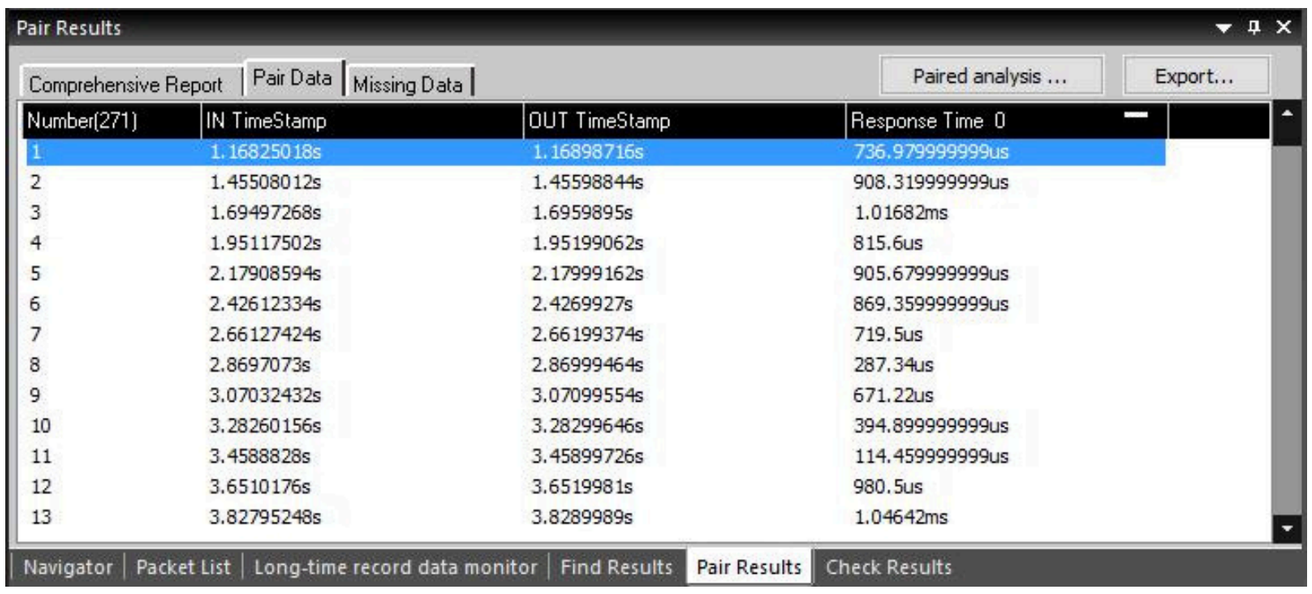


ADVANCED TIMING & PERFORMANCE STATISTICS

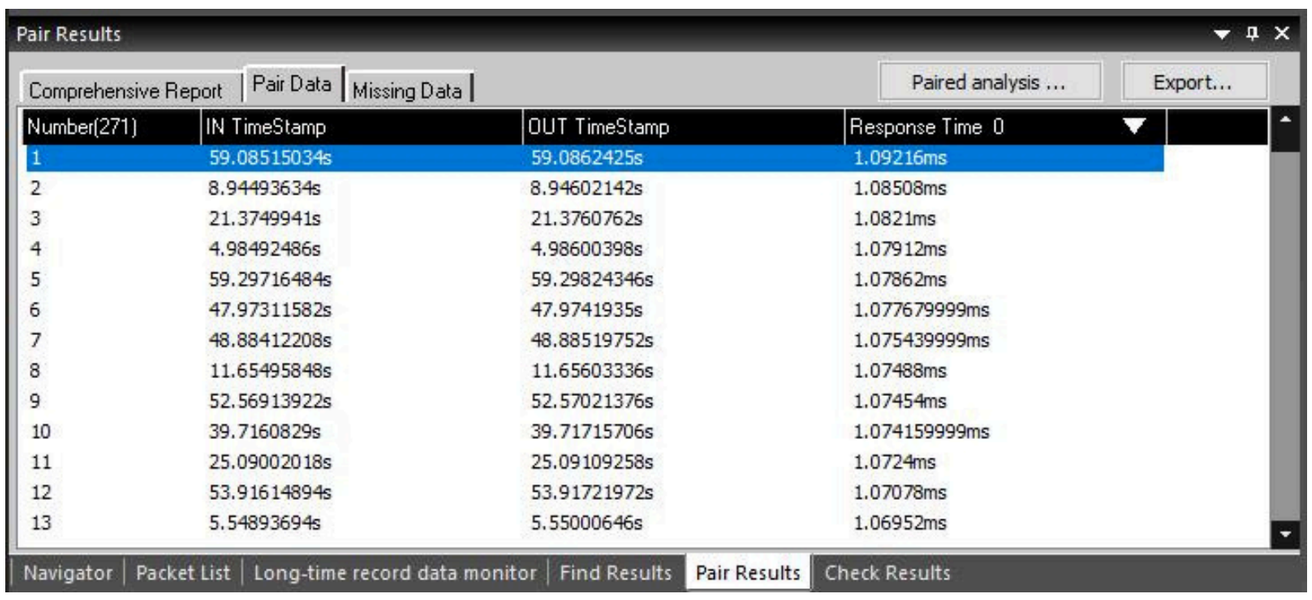
Based on the processed measurement data, the software has identified 2 valid results matching the predefined criteria.



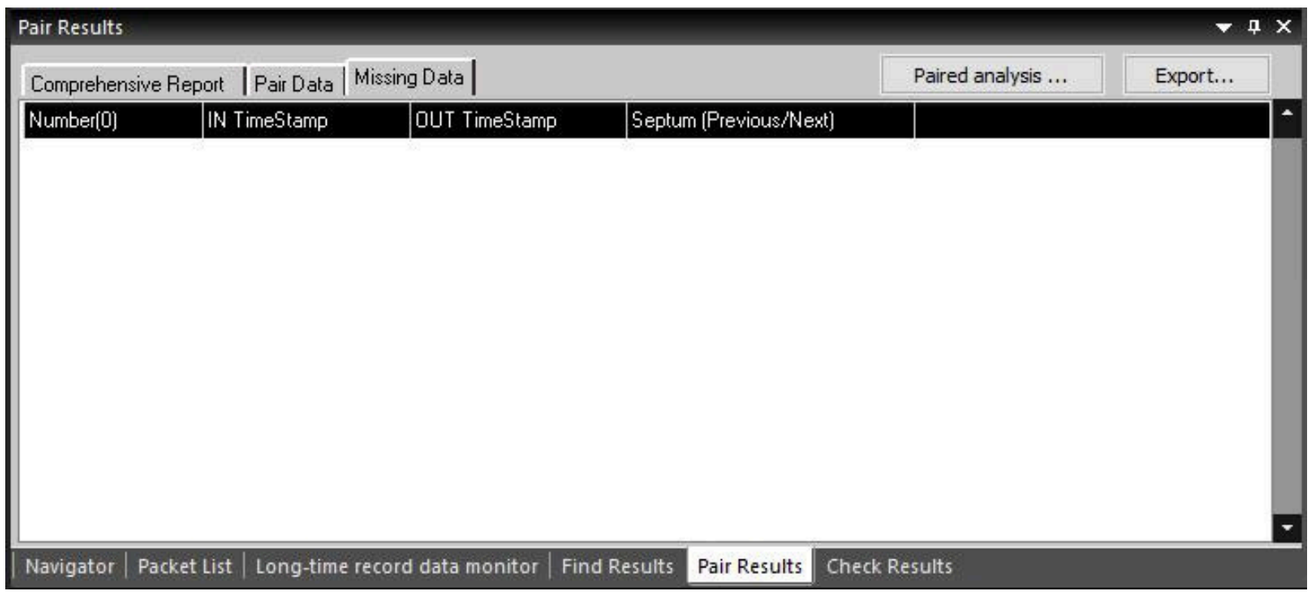
Average & Max. Software Interface



Response Time Software Interface



Sorting Software Interface

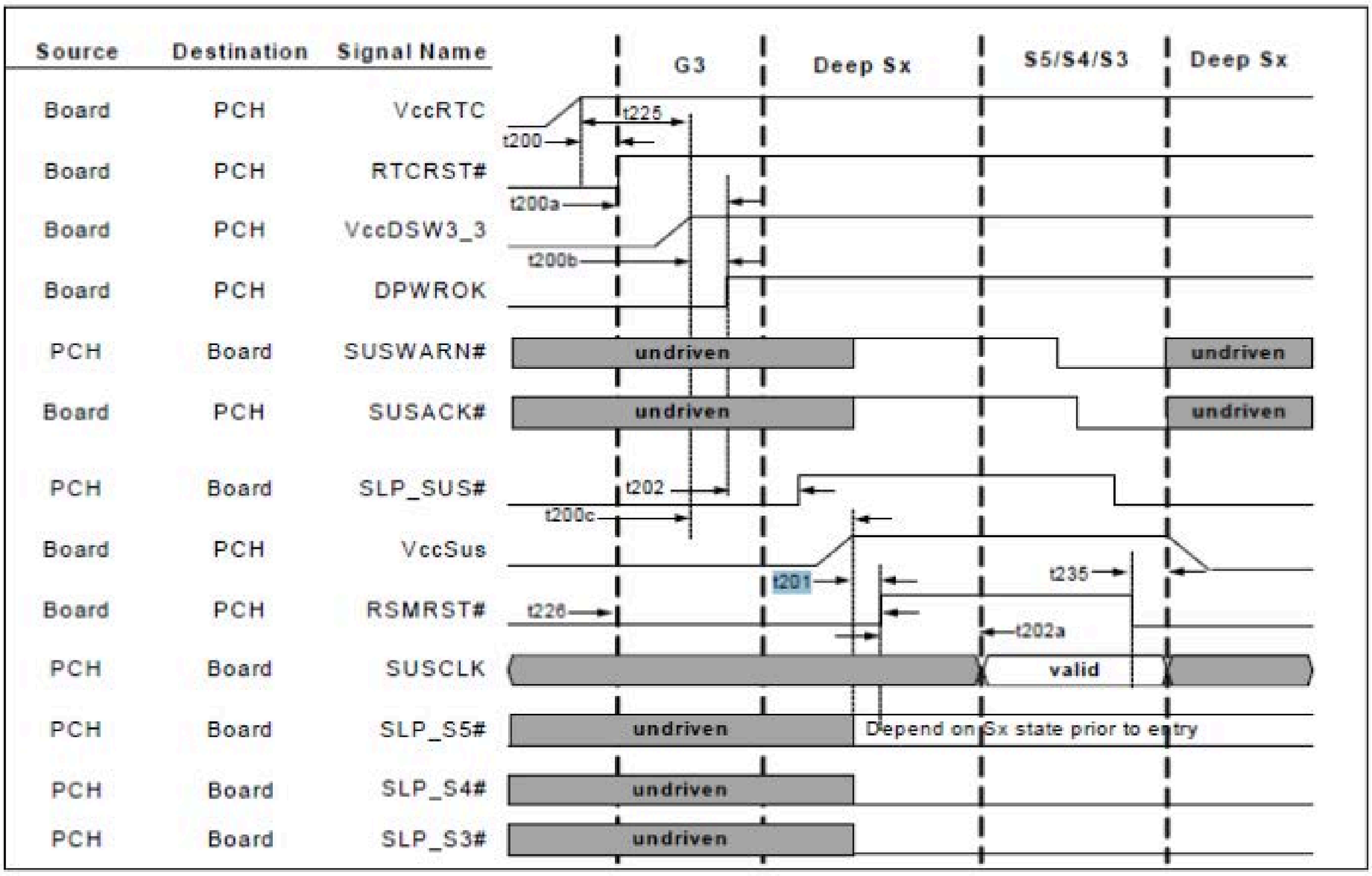


Missing Software Interface

KEY SPECIFICATIONS

COMPLIANCE VALIDATION (PASS/FAIL)

On a Deep Sx supported platform, platform must transition to Sx state upon G3 exit, prior to determining that conditions are met for a Deep Sx transition (G3->Sx->Deep Sx).



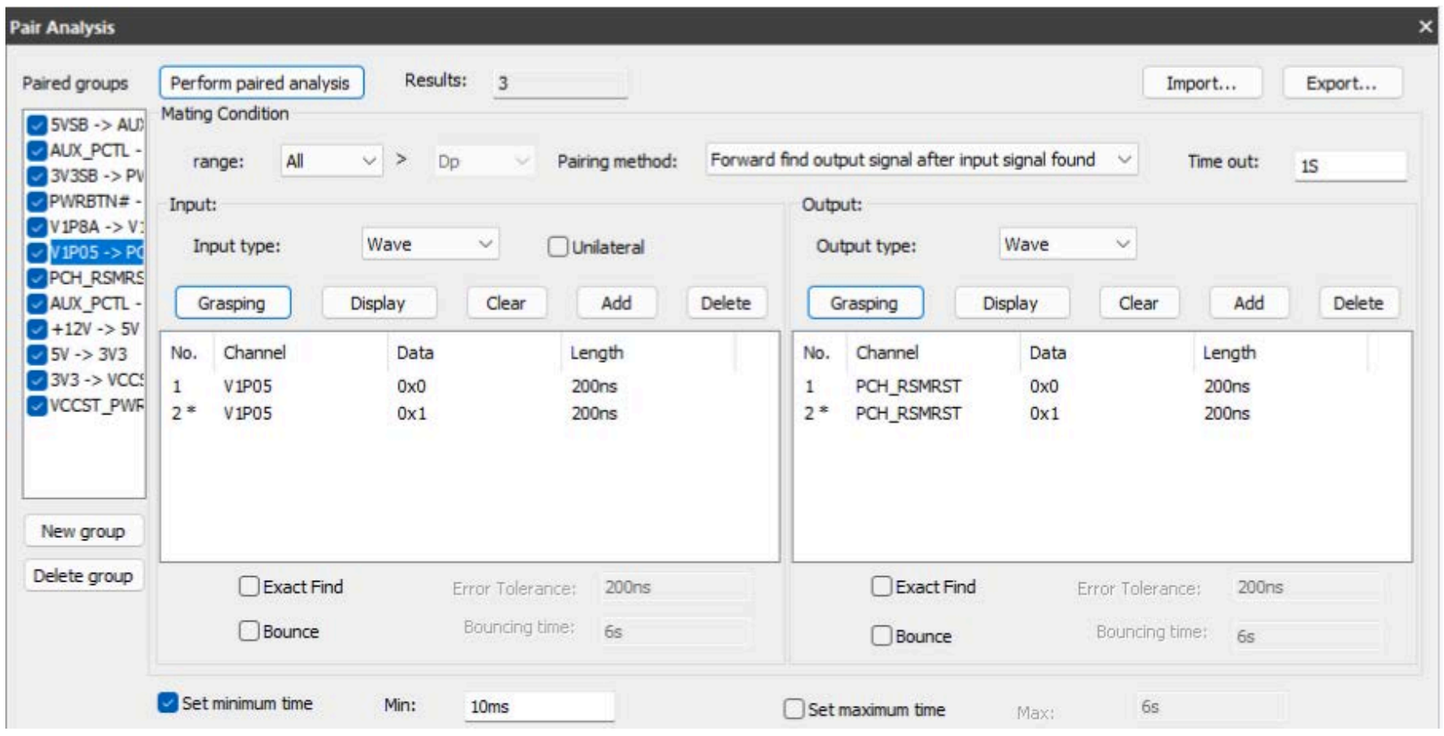
Timing Constraint Verification The following figure illustrates the timing requirements between Vccsus and RSMRST# signals (where Vccsus must transition high prior to RSMRST#). Users can define these specifications within the ProCision software to automatically analyze and verify if the signal sequences comply with power-on sequence standards.

Sym	Parameter	Min	Max	Units	Notes	Fig
t200b	VccDSW3_3 active to DPWROK high	10	—	ms		8-1, 8-2
t200c	VccDSW3_3 active to VccSus3_3 active	0	—	ms		8-1, 8-2
t201	VccSUS active to RSMRST# de-assertion	10	—	ms	1	8-1, 8-2

Reference Specification for T201 Timing Parameters This excerpt from the datasheet provides the specific timing values required to fulfill the T201 constraint mentioned above.

KEY SPECIFICATIONS

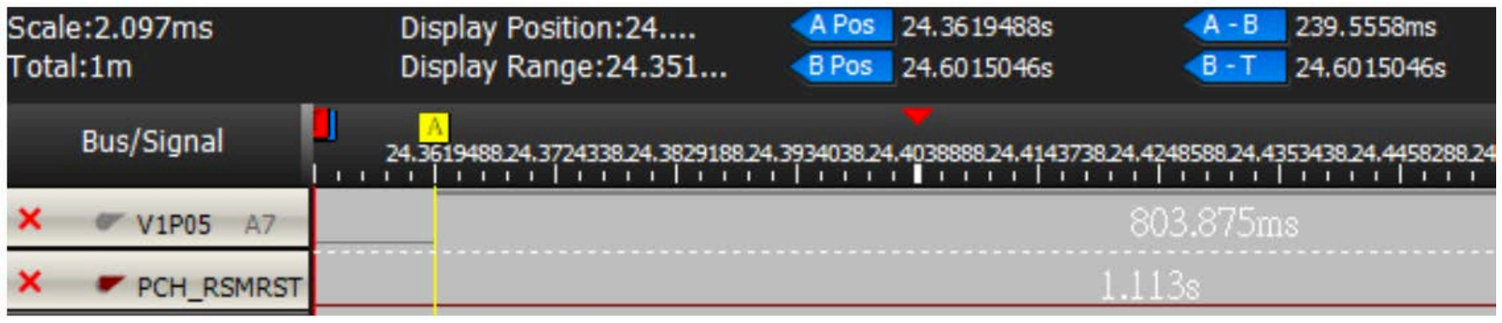
COMPLIANCE VALIDATION (PASS/FAIL)



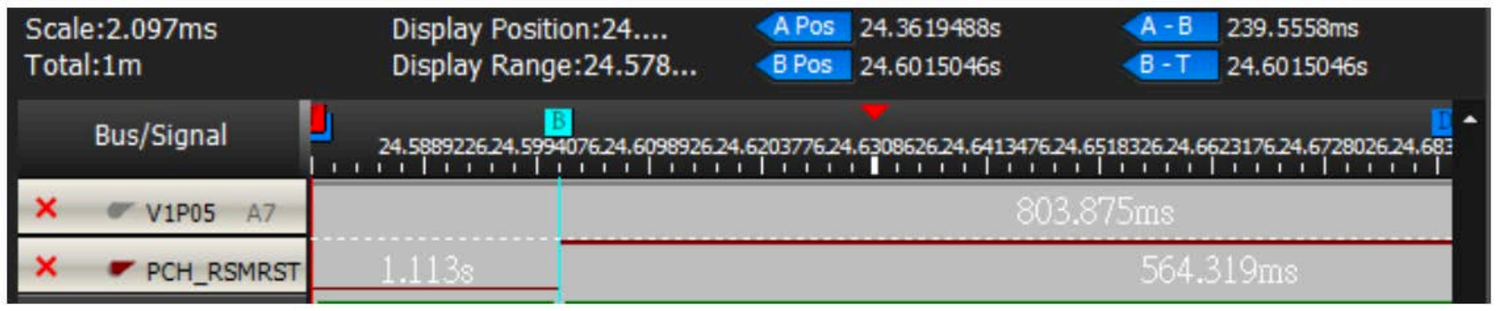
Configuring Timing Analysis Parameters

Based on the timing requirements shown above, the V1P05 and PCH_RSMRST channels on the ProCision interface correspond to Vccsus and RSMRST# in the reference specification. The timing constraint T201 represents the interval between the rising edge of Vccsus and the rising edge of RSMRST#.

The figure below illustrates the software configuration: the Input Channel is filtered to V1P05, and the Output Channel is filtered to PCH_RSMRST. The "Set Minimum Time" is defined as 10 ms, directly adhering to the minimum specification (Min = 10ms) defined for T201 in the supplemental timing table.



Vccsus (V1P05) Rising Edge Waveform, Software Interface



PCH_RSMRST# Rising Edge Waveform, Software Interface

Check Results

Comprehensive Report

Group	Minimum response Min.Time	Maximum Response Max.Time	Check Results
Summary	--	--	Pass
5VSB -> AUX_PCTL	116us	116us	Pass
AUX_PCTL -> 3V3SB	43.847ms (0ms)	43.847ms	Pass
3V3SB -> PWRBTN#	1.799ms	1.8154ms	Pass
PWRBTN# -> V1P8A	1.6898ms	1.7118ms (500ms)	Pass
V1P8A -> V1P05	11.232ms (0ms)	11.321ms	Pass
V1P05 -> PCH_RSMRST	239.1964ms (10ms)	239.5558ms	Pass
PCH_RSMRST -> AUX_PCTL	2.2400218s (100ms)	2.2400902s	Pass
AUX_PCTL -> +12V	72.8704ms	77.003ms (500ms)	Pass
+12V -> 5V	643.6us (0ms)	651.6us	Pass
5V -> 3V3	279us (0ms)	287us	Pass
3V3 -> VCCST_PWRGD	267.1378ms (10ms)	273.4536ms	Pass
VCCST_PWRGD $\rightarrow$ PC...	0ns	0ns	Pass

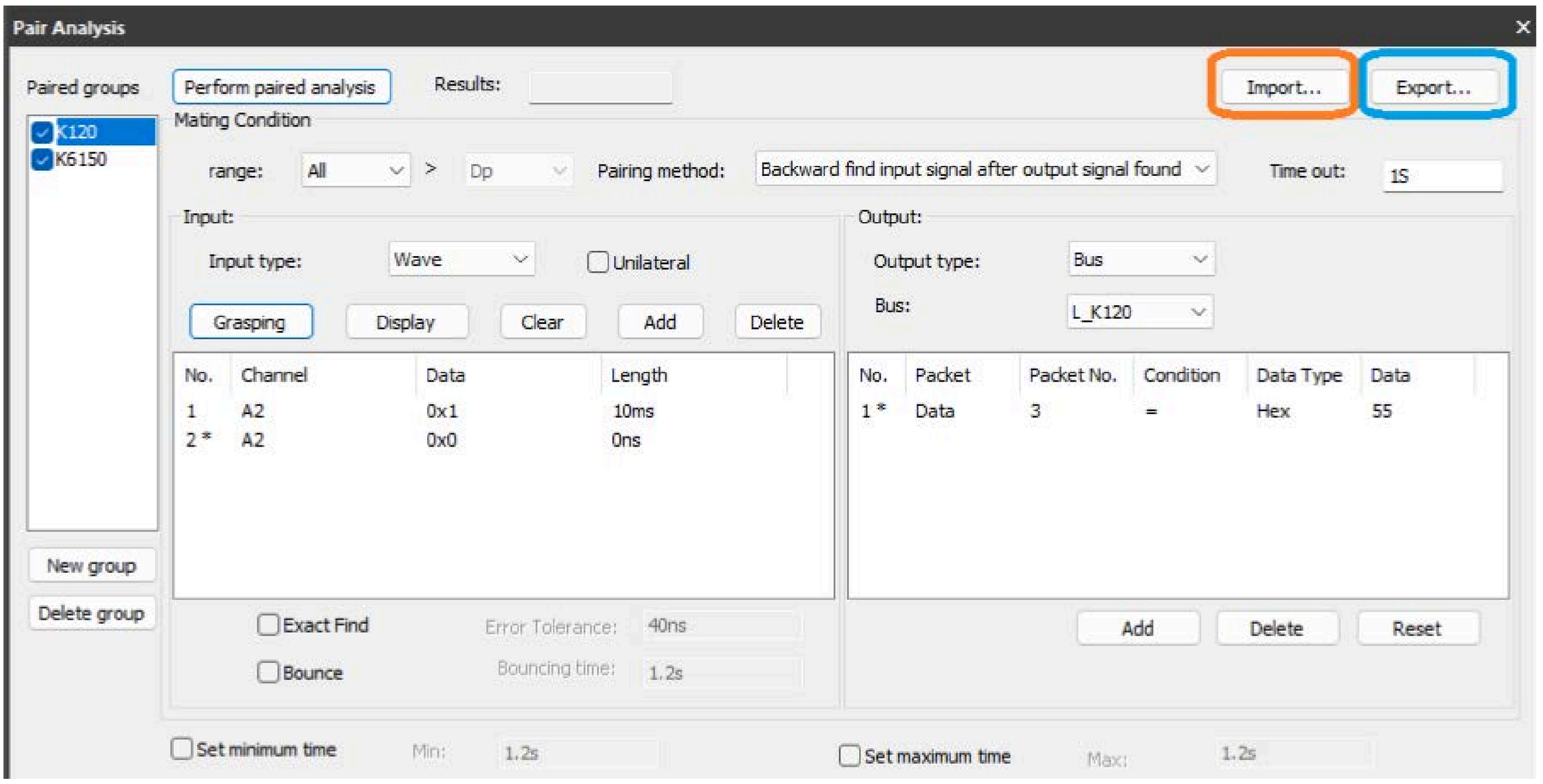
Navigator | Packet List | Long-time record data monitor | Find Results | Pair Results | Check Results

Both data points exceed the 10 ms minimum threshold. As the measured values are greater than the specified Min value, the results are deemed compliant and marked as PASS.

KEY SPECIFICATIONS

SCRIPTING: REUSABLE FUNCTIONALITY

User-defined settings can be seamlessly migrated between data files via Import/Export functionality. This allows for the rapid replication of test conditions across similar product lines, eliminating redundant setups and significantly reducing time-to-analysis.

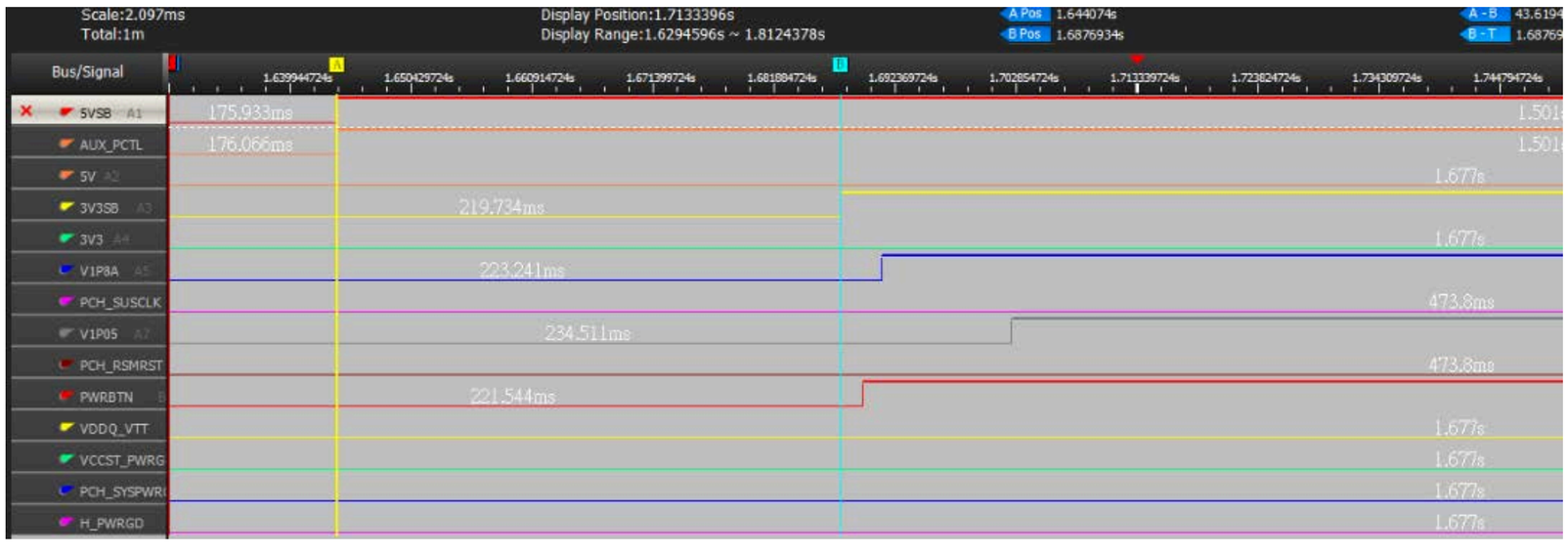


32-CHANNEL SYNCHRONOUS MEASUREMENT

Capture all power rails and control signals in a single boot-up cycle. This ensures comprehensive Power Sequencing validation in full compliance with chipset timing specifications.

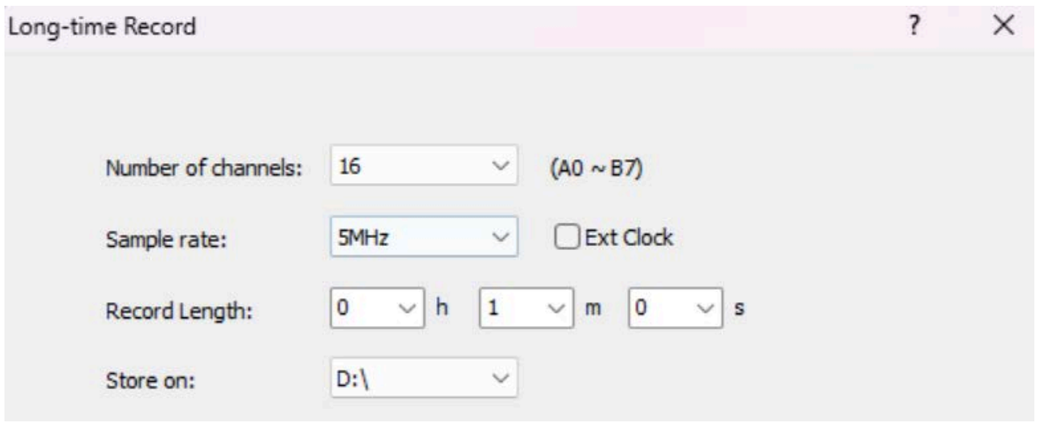
Hardware Interfaces

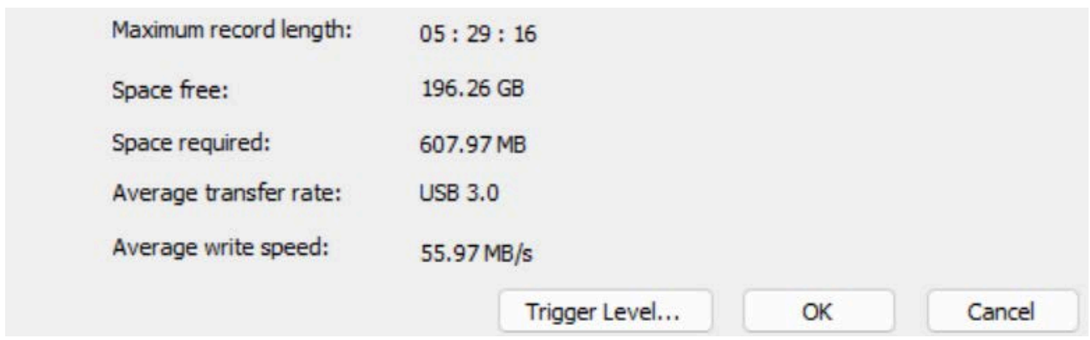
Software Interface



KEY SPECIFICATIONS

LONG-TIME RECORD

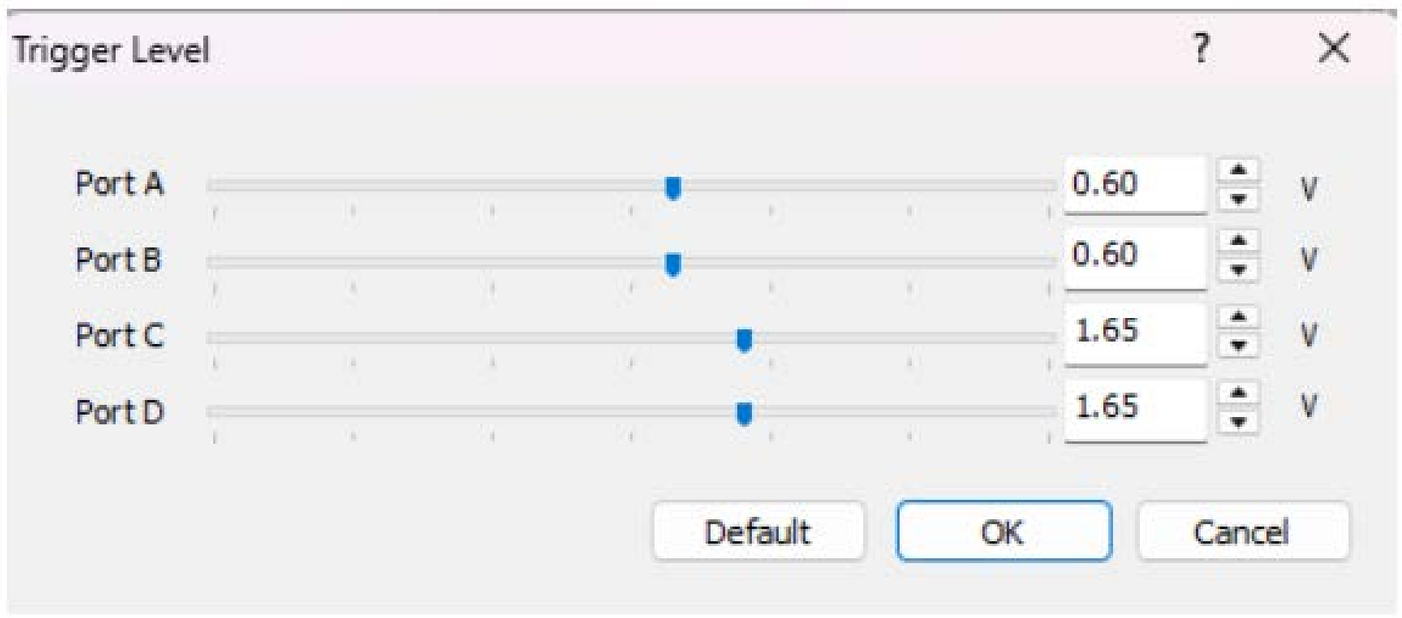




- Continuous Data Streaming: Leverage the LAP-C Pro's advanced Data Streaming technology to bypass traditional hardware memory limits. Capture digital signals continuously for hours or even days directly to your PC storage.
- Precision Timing & Zero Data Loss: Maintain high-speed sampling integrity during extended recording sessions via USB 3.0 high-speed transmission, ensuring that even the most elusive transient faults are captured in full detail.
- Scalable Storage Architecture: Utilize your PC's HDD/SSD capacity to store massive logic data, eliminating buffer overflow issues common in traditional standalone logic analyzers.

LOW-VOLTAGE TRIGGER OPTIMIZATION

Specifically engineered for low-voltage domains (e.g., 1.05V), the system allows for an optimized trigger threshold between 0.5V and 0.6V, ensuring precise capture of critical logic transitions.



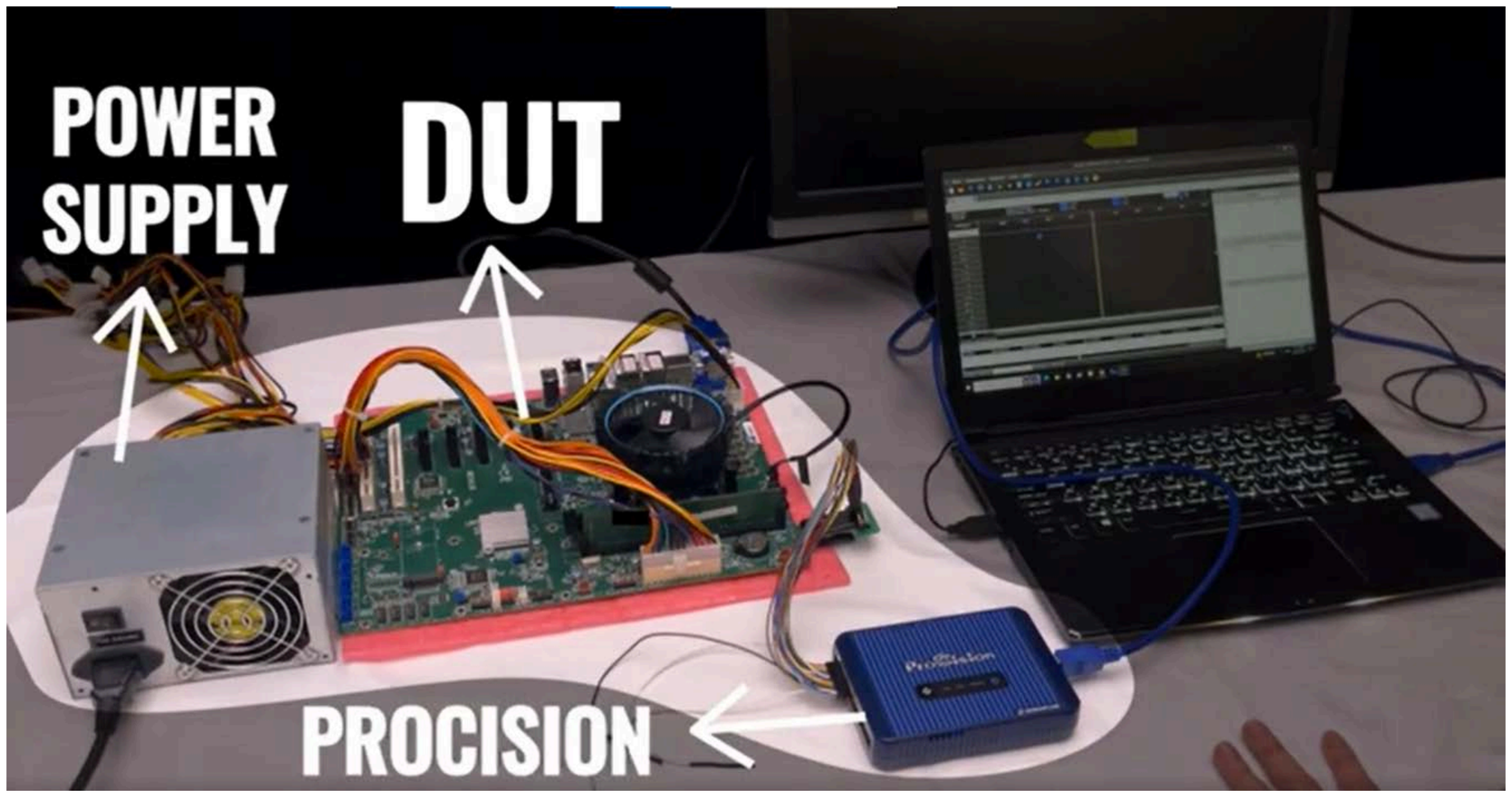
Trigger Level Software Interface

Trigger Level	User-defined
Trigger Level Range	-6 to 6V
Trigger Level Resolution	10mV/STEP
Reference Level Accuracy	±100mV+5%Vth
Input DC V (Max)	±30 V

Trigger Level Technical Specifications

CASE STUDIES

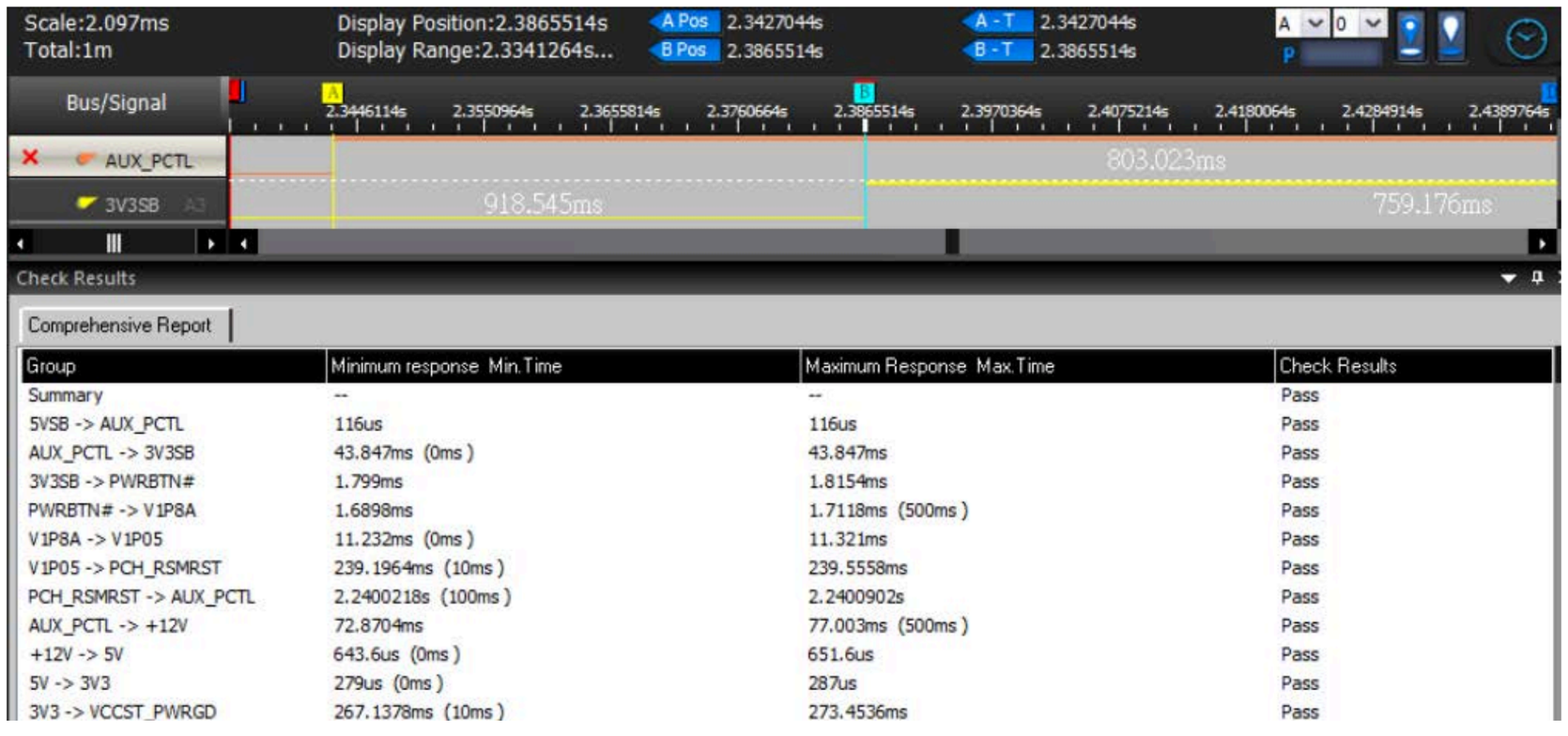
THE POWER SEQUENCING OF INTEL-CHIPSET MOTHERBOARDS



Hardware Configuration and Test Environment

Device Under Test: Industrial-grade motherboard

Complete Process: Covering the entire sequence from power-on to BIOS screen display



Group	Minimum response Min.Time	Maximum Response Max.Time	Check Results
Summary	--	--	Pass
5VSB -> AUX_PCTL	116us	116us	Pass
AUX_PCTL -> 3V3SB	43.847ms (0ms)	43.847ms	Pass
3V3SB -> PWRBTN#	1.799ms	1.8154ms	Pass
PWRBTN# -> V1P8A	1.6898ms	1.7118ms (500ms)	Pass
V1P8A -> V1P05	11.232ms (0ms)	11.321ms	Pass
V1P05 -> PCH_RSMRST	239.1964ms (10ms)	239.5558ms	Pass
PCH_RSMRST -> AUX_PCTL	2.2400218s (100ms)	2.2400902s	Pass
AUX_PCTL -> +12V	72.8704ms	77.003ms (500ms)	Pass
+12V -> 5V	643.6us (0ms)	651.6us	Pass
5V -> 3V3	279us (0ms)	287us	Pass
3V3 -> VCCST_PWRGD	267.1378ms (10ms)	273.4536ms	Pass

Intuitive Measurement Results and Report Generation

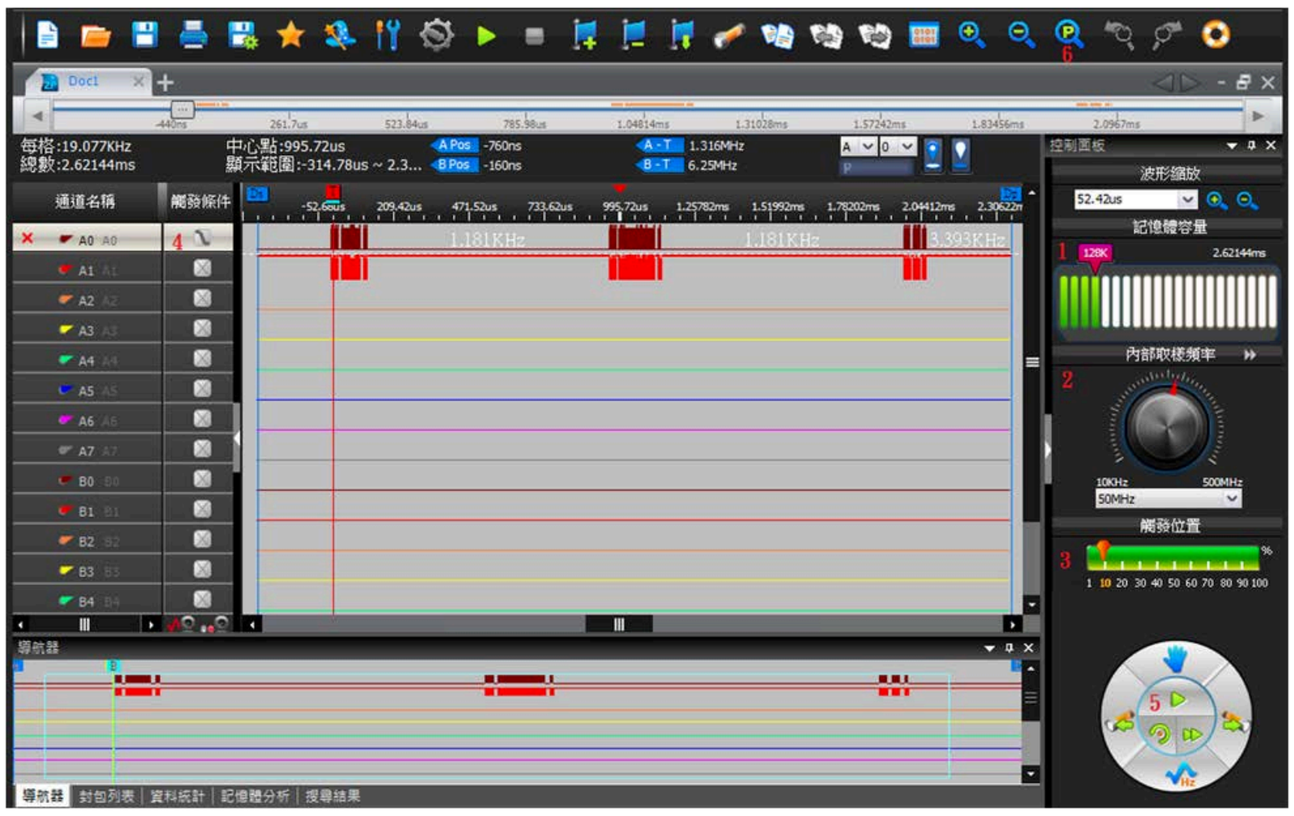
Automatic Interval Identification: Software calculates signal intervals and displays them in a graphical interface.

Quick Overview (Check Results): Pass/Fail judgments are shown clearly, with abnormal values auto-annotated (e.g., spec limits), reducing comparison time.

Modular Configuration: One setup works across same-generation processors, offering strong scalability.

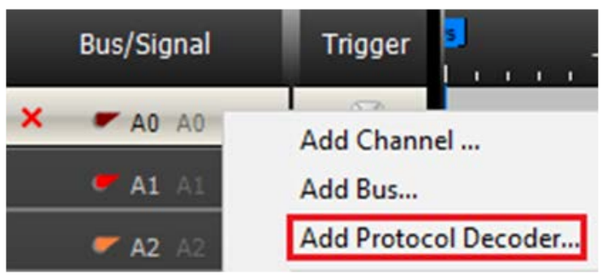
CASE STUDIES

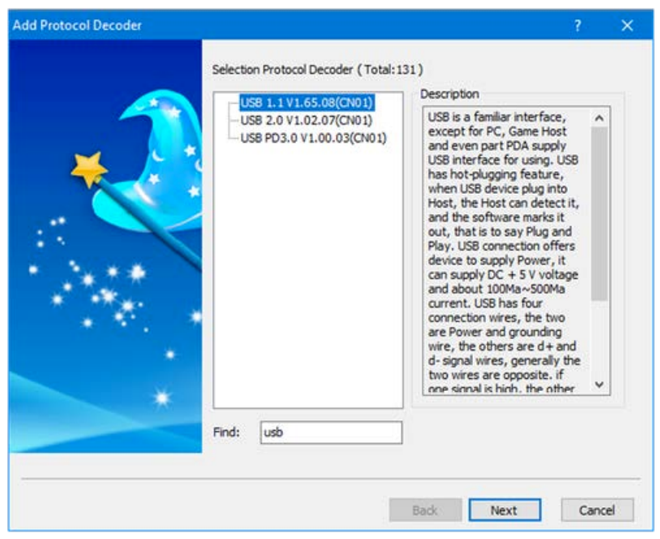
136 PROTOCOL DECODING APPLICATIONS： USB1.1 UART

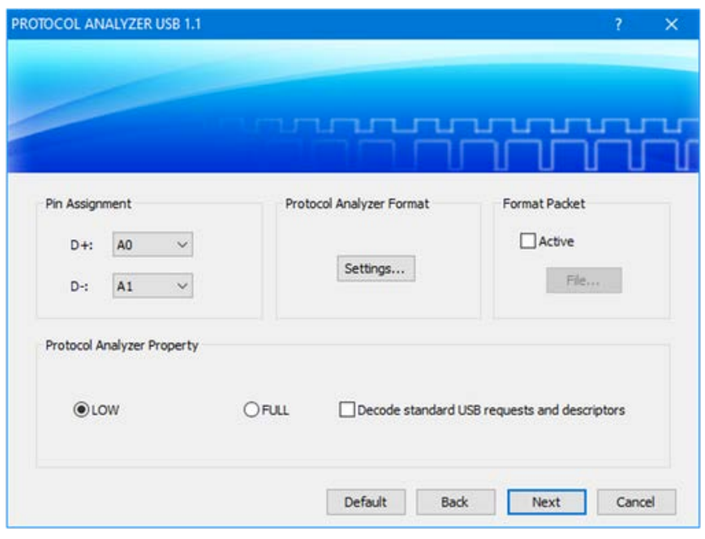


Acquisition Settings:

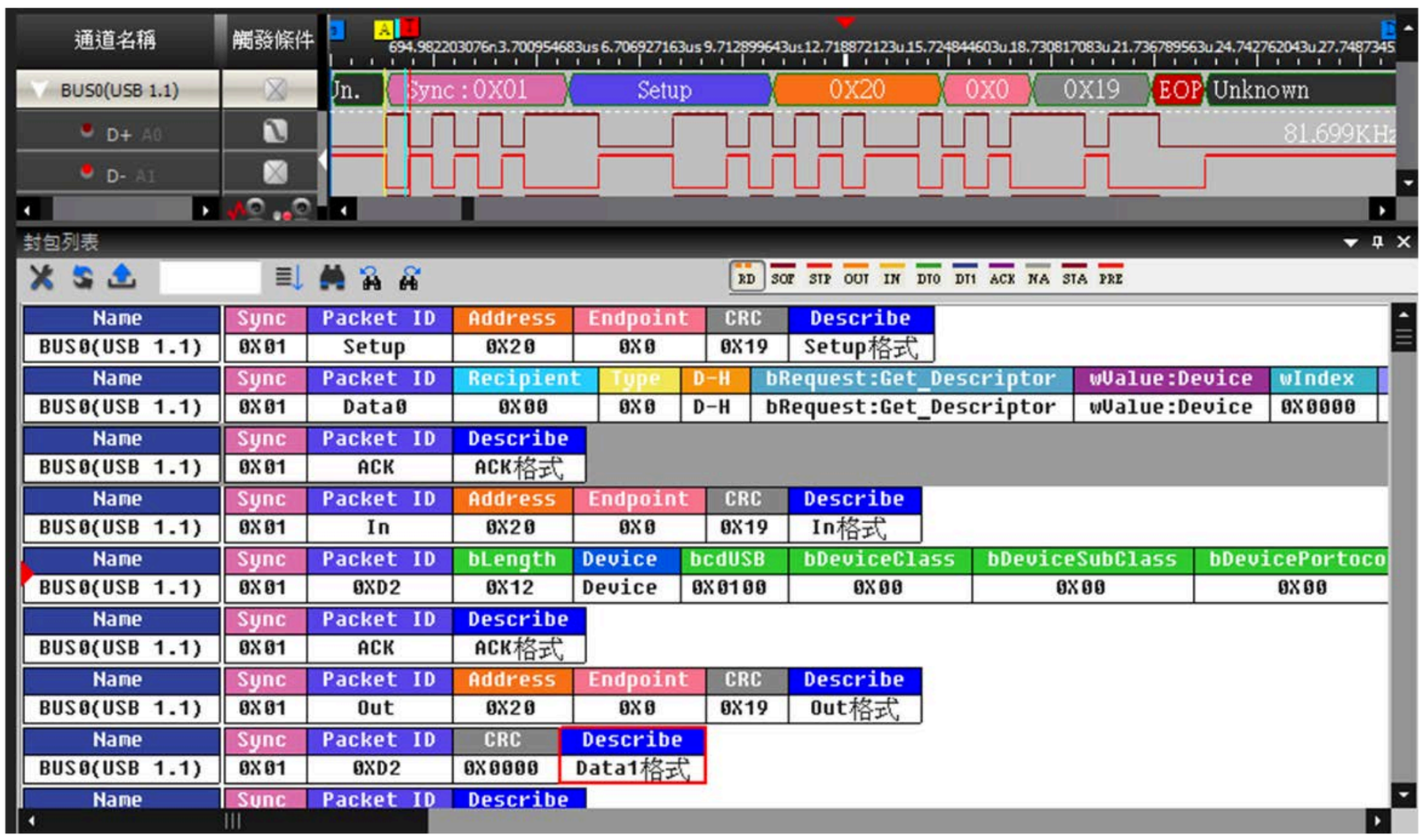
- Trigger Condition: Channel A0 Falling Edge (A0 ↓)
- Sampling Rate: 50 MHz / 100 MHz







- Streamline bus configuration with an integrated search function. Simply enter keywords like "USB" to quickly locate and deploy specific protocol decoders.



- USB 1.1 Packet List Example

PROTOCOL DECODING SPECIES (FREE)

AUTOMOTIVE

·CAN 2.0B	·CAN FD	·DSI Bus	·FlexRay 2.1A
·LIN 2.2A	·MVB	·PSI5	·SENT
·WTB			

PC SYSTEM

·AMD_SVI2	·DDC EDID	·eSPI	·FWH
·GPIB	·HID Over I2C	·I80	·IDE
·Low Pin Count	·LPC-SERIRQ	·LPT	·PCI
·PECI	·PS/2	·Serial GPIO IBPI	·SVID
·USB 1.1	·USB 2.0	·USB PD3.0	

IC INTERFACE

·1-WIRE	·1-Wire(Advanced)	·3-WIRE	·BDM
·BiSS C	·HPI	·I2C	·I3C
·JTAG 2.0	·MCU-51 DECODE	·MDDI	·MICROWIRE
·SDI-12	·Serial Wire Debug(SWD)	·SLE4442	·SPI
·SPI PLUS	·SSI Interface	·ST7669	·UART(RS-232C/422/485)

DIGITAL AUDIO

·AC97	·AES_EBU	·DP AUX Channel 1.1	·DSA Interface
·HD Audio	·HDMI CEC	·I2S	·MHL-CBUS
·MIDI	·MIPI_CSI-2	·MIPI DSI	·PCM
·PDM	·PSB Interface	·S/PDIF	·SoundWire
·STBus			

BASIC LOGIC APPLICATION

·ARITHMETICAL LOGIC	·DIGITAL LOGIC	·JK FLIP-FLOP	·UP DOWN COUNTER

MEMORY

·Compact Flash 4.1	·eMMC	·I2C(EEPROM 24L)	·I2C(EEPROM 24LCS61/24LCS62)
·MICROWIRE(EEPROM 93C)	·Quad SPI	·SAMSUNG K9(NAND Flash)	·SD2.0/SDIO
·SD3.0	·SDIO3.0	·S29GL	·SPI Compatible(Atmel Memory)
·UNI/O			

OPTOELECTRONICS

·7-SEGMENT LED	·CCIR601	·CCIR656	·CMOS IMAGE
·DALI Interface	·DM114/DM115	·DMX512	·LCD1602
·LCD12864	·LED Pitch Array	·LG4572	·RGB Interface
·S2Cwire/AS2Cwire	·SCCB		

INFRARED RAYS

·IRDA	·NEC PD6122	·Philips RC-5	·Philips RC-6
·PT2262/PT2272			

POWER

·BMS	·HDQ	·PMBus 1.1	·QI
·SDQ	·SMBus 2.0		

WIRELESS

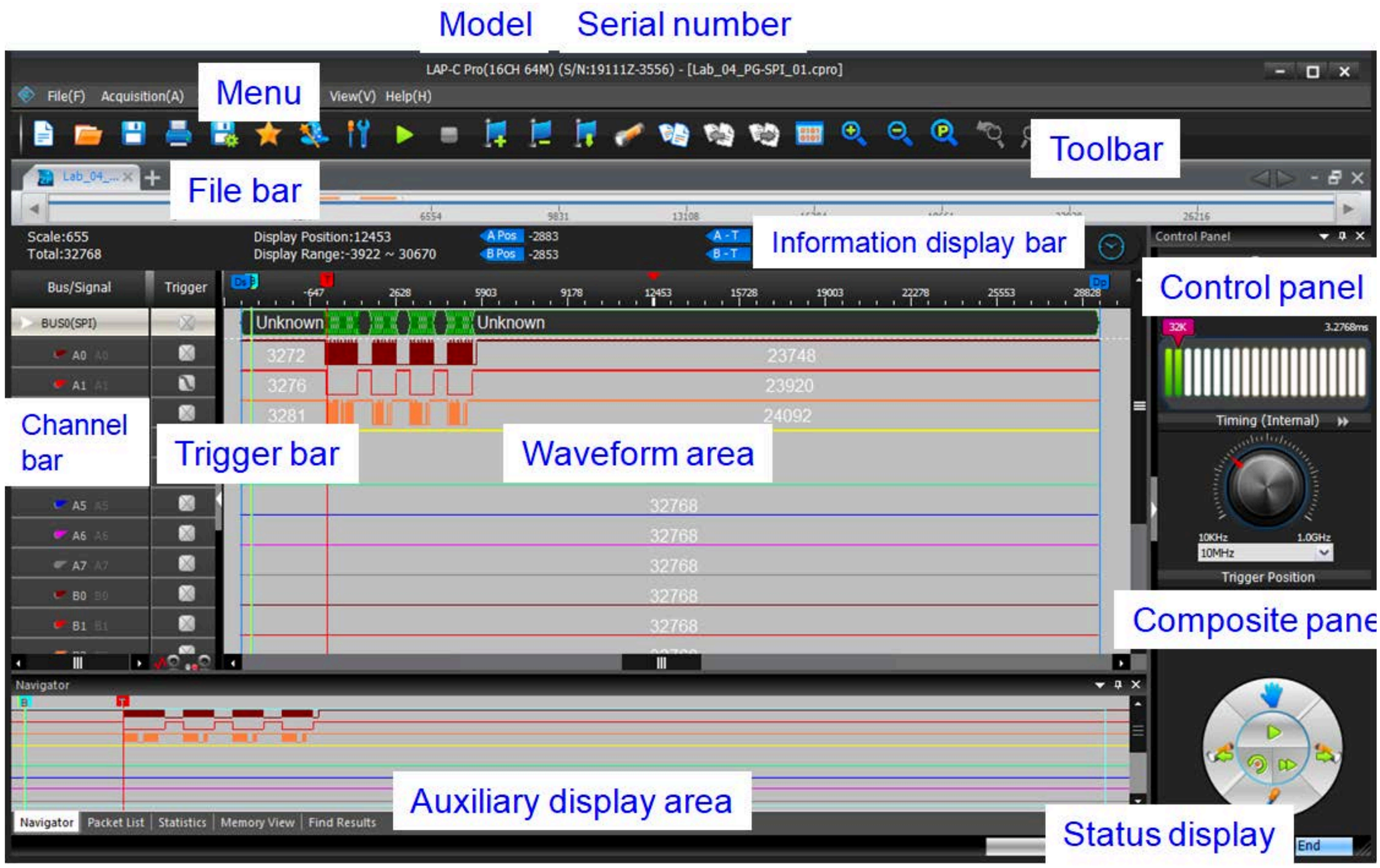
·Differential Manchester	·DigRF	·ISO7816 UART	·KEELOQ Code Hopping
·MANCHESTER	·MII	·MILLER	·MIL-STD-1553
·MIPI RFFE	·MODIFIED MILLER	·SIGNIA 6210	·SWP
·WIEGAND	·WWV/WWVH/WWVB		

OTHER

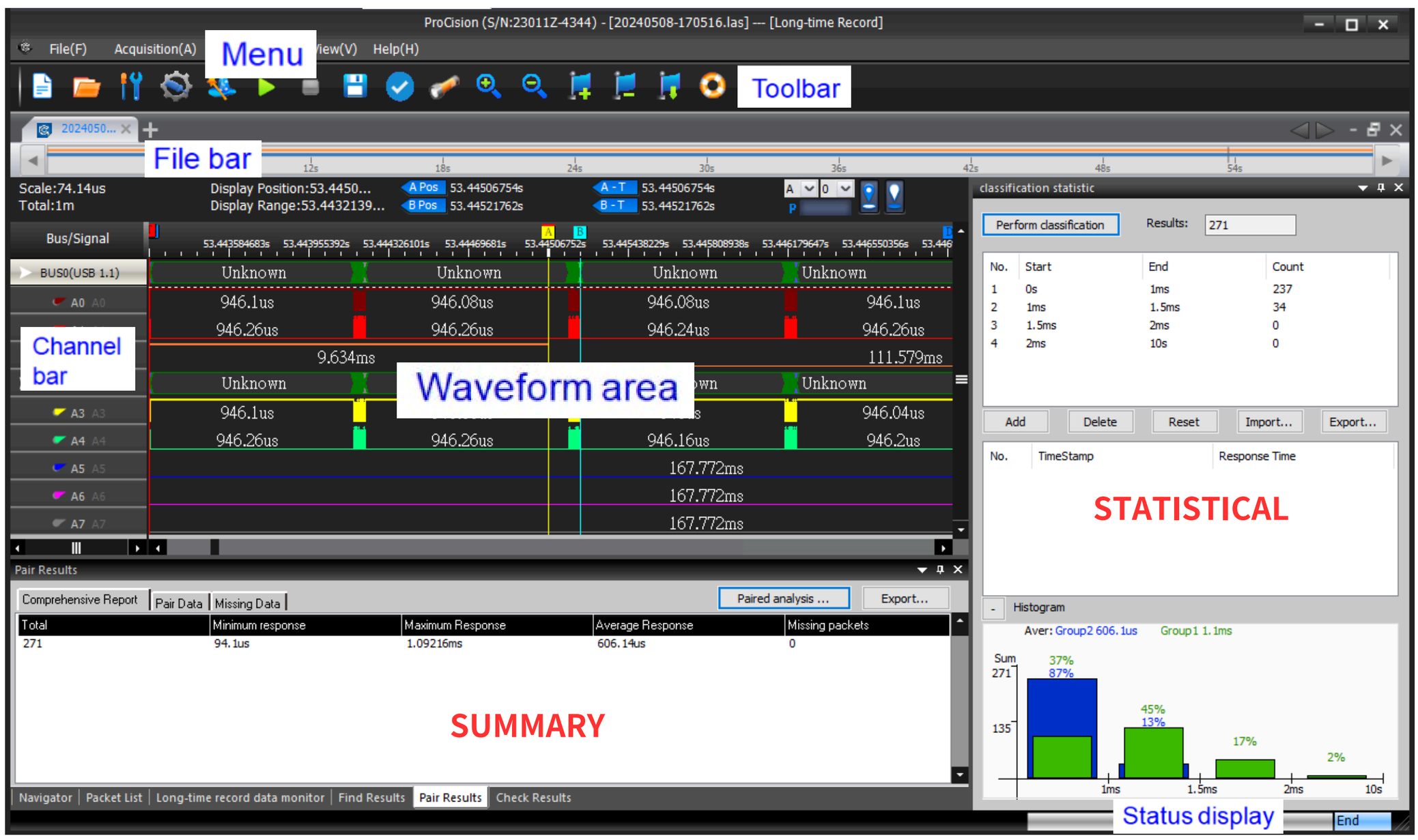
·DS1302	·DS18B20	·EtherCAT	·HART
·HDLC	·IO-Link	·KNX	·Line Code
·ModBus	·MODIFIED SPI	·OPENTHERM 2.2	·PROFIBUS
·SHT11	·YK-5		

UI & UX

SOFTWARE INTERFACE



SOFTWARE INTERFACE



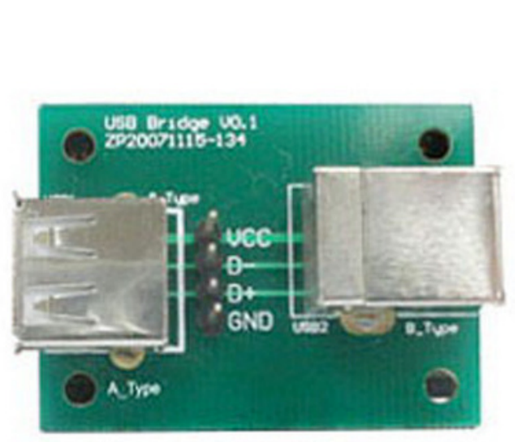
STANDARD PACKAGE

PACKAGE CONTENTS

STANDARD ACCESSORIES INCLUDED:

ProCision Main Unit

USB 3.0 Interface Cable



USB 1.1 measurement fixture x2

10 channel testing cable package(10cm) x4

10 channel testing cable package(25cm) x4

1 pin test lead (black)

1 pin test lead (gray) x4

Probe Clip-on Hook (20 pcs * 2 pack)

Carry Bag

CONTACT & SUPPORT

AFTER-SALES SERVICE & WARRANTY

We provide comprehensive technical support and a 2-year limited warranty to ensure your equipment operates at peak performance. For repair services or hardware calibration, please contact our authorized service centers.

TECHNICAL SUPPORT QR CODE

Email: service@zeroplus.com.tw
Web: https://www.zeroplus.com.tw/logic-analyzer_en/

V26.03